

1 CLAIMS

2 We claim:

3 1. An apparatus for switching packets, each packet having a header
 4 portion, an optional corresponding tail portion, and a class of service indicator, said
 5 apparatus comprising:
 6 a pipelined switch comprising:
 7 a plurality of packet header buffers (PHBs);
 8 an equal plurality of PHB pointers, each said PHB pointer pointing to a
 9 corresponding PHB; and
 10 an equal plurality of pipeline stage circuits connected in a sequence,
 11 comprising at least a first stage circuit and a last stage circuit,
 12 wherein:
 13 each said stage circuit begins an operation substantially
 14 simultaneously with each other;
 15 each said stage circuit passes data to a next stage circuit in said
 16 sequence when every said operation performed by all
 17 said stage circuits is completed;
 18 said first stage circuit reads said header portion and stores said
 19 header portion in said corresponding PHB using said
 20 corresponding PHB pointer; and
 21 said last stage circuit outputs a modified header portion; and
 22 a receive buffer manager (RBM) comprising:
 23 a joining circuit connected to said pipelined switch wherein said
 24 modified header portion and said corresponding tail portion are
 25 joined to form a modified packet;
 26 a receive queue manager connected to said joining circuit that buffers
 27 said modified packet in a receive packet buffer and enqueues
 28 said modified packet using said class of service indicator and a
 29 plurality of receive queues; and

1 a dequeue circuit connected to said receive queue manager and said
 2 receive packet buffer, wherein said dequeue circuit uses said
 3 class of service indicator to dequeue said modified packet to a
 4 switch fabric.

5 2. The apparatus as recited in Claim 1, wherein said plurality of pipeline
 6 stage circuits further comprise:

7 a pre-process circuit connected to said first stage circuit, wherein said pre-
 8 process circuit uses a second said PHB pointer to record first data in
 9 said corresponding PHB;

10 a pointer lookup circuit connected to said pre-process circuit that compares
 11 said header portion to a first data structure and determines a leaf
 12 pointer using said second PHB pointer;

13 a table lookup circuit connected to said pointer lookup circuit that uses said
 14 leaf pointer to access one or more sets of linked data structures and to
 15 fetch second data, wherein said table lookup circuit uses a third said
 16 PHB pointer to record said second data in said corresponding PHB;
 17 and

18 a post-process circuit using said third PHB pointer and connected to said table
 19 lookup circuit, wherein said post-process circuit uses a fourth said PHB
 20 pointer to record third data in said corresponding PHB;

21 wherein said last pipeline stage circuit comprises a gather circuit connected to said
 22 post-process circuit, and wherein said gather circuit uses said fourth PHB pointer to
 23 assemble said modified header portion.

24 3. The apparatus as recited in Claim 1, further comprising:

25 an input device that receives said packet; and

26 a first buffer connected between said input device and said first stage circuit,
 27 wherein said first buffer buffers said header portion and said tail
 28 portion.

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a dequeue circuit connected to said transmit queue manager and said transmit packet buffer, wherein said dequeue circuit uses said class of service indicator to dequeue each said packet.

12. The apparatus as recited in Claim 11, wherein said transmit packet buffer comprises buffers of different sizes.

13. The apparatus as recited in Claim 11, wherein said transmit packet buffer comprises buffers of equal size.

14. The apparatus as recited in Claim 11, wherein said transmit queue manager comprises a congestion avoidance circuit utilizing a status of each said transmit queue.

15. The apparatus as recited in Claim 14, wherein said status comprises a measure of average queue depth.

16. The apparatus as recited in Claim 11, further comprising a transmit FIFO connected to an output of said dequeue circuit.

17. An apparatus for switching packets in a communications network device comprising:
a buffer that receives one or more packets, said packets comprising a class of service indicator;
a transmit queue manager connected to said buffer that buffers each said packet in a transmit packet buffer and enqueues said packet using said class of service indicator and a plurality of transmit queues; and
a dequeue circuit connected to said transmit queue manager and said transmit packet buffer, wherein said dequeue circuit uses said class of service indicator to dequeue each said packet.

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22. The apparatus as recited in Claim 17, further comprising a transmit FIFO connected to an output of said dequeue circuit.

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1 38. The method of Claim 35, wherein said buffering further comprises
2 avoiding congestion using a status of each said queue.

3 39. The method of Claim 38, wherein said status comprises a measure of
4 average queue depth.

5 40. The method of Claim 35, wherein said dequeuing uses a transmit FIFO.
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8 41. A computer system for interfacing with a communications network,
9 comprising computer instructions for:
10 receiving a packet, said packet having a header portion, an optional
11 corresponding tail portion, and a class of service indicator;
12 switching said packet through a pipelined switch having a plurality of packet
13 header buffers (PHBs), an equal plurality of PHB pointers wherein
14 each said PHB pointer points to a corresponding PHB, and an equal
15 plurality of pipeline stages connected in a sequence, comprising at least
16 a first stage and a last stage, said switching further comprising:
17 beginning said sequence in each said stage substantially simultaneously
18 with each other said stage;
19 passing data to a next stage circuit in said sequence when every said
20 operation performed by all said stage circuits is completed;
21 reading and storing said header in said corresponding PHB using said
22 corresponding PHB pointer; and
23 outputting a modified header portion; and
24 buffering said modified header portion in a receive buffer manager (RBM),
25 said buffering further comprising:
26 joining said modified header portion and said corresponding tail
27 portion to form a modified packet;
28 buffering and enqueueing said modified packet using said class of
29 service indicator; and

dequeueing said modified packet using said class of service indicator.

42. The computer system of Claim 41, wherein said switching further comprises:

- recording first data in said corresponding PHB using a second said PHB pointer;
- comparing said header portion to a first data structure and determining a leaf pointer using said second PHB pointer;
- fetching second data using said leaf pointer to access one or more sets of linked data structures and recording said second data in said corresponding PHB using a third said PHB pointer;
- post-processing said header portion using said third PHB pointer and recording third data in said corresponding PHB using a fourth said PHB pointer;
- and
- assembling said modified header portion using said fourth PHB pointer.

43. The computer system of Claim 41, further comprising:

- receiving one or more packets;
- buffering and enqueueing each said packet using said class of service indicator and a plurality of queues; and
- dequeueing each said packet using said class of service indicator.

44. A computer readable storage medium, comprising computer instructions for:

- receiving a packet, said packet having a header portion, an optional corresponding tail portion, and a class of service indicator;
- switching said packet through a pipelined switch having a plurality of packet header buffers (PHBs), an equal plurality of PHB pointers wherein each said PHB pointer points to a corresponding PHB, and an equal

plurality of pipeline stages connected in a sequence, comprising at least a first stage and a last stage, said switching further comprising: beginning said sequence in each said stage substantially simultaneously with each other said stage; passing data to a next stage circuit in said sequence when every said operation performed by all said stage circuits is completed; reading and storing said header in said corresponding PHB using said corresponding PHB pointer; and outputting a modified header portion; and buffering said modified header portion in a receive buffer manager (RBM), said buffering further comprising: joining said modified header portion and said corresponding tail portion to form a modified packet; buffering and enqueueing said modified packet using said class of service indicator; and dequeuing said modified packet using said class of service indicator.

45. The computer readable storage medium of Claim 44, wherein said switching further comprises: recording first data in said corresponding PHB using a second said PHB pointer; comparing said header portion to a first data structure and determining a leaf pointer using said second PHB pointer; fetching second data using said leaf pointer to access one or more sets of linked data structures and recording said second data in said corresponding PHB using a third said PHB pointer; post-processing said header portion using said third PHB pointer and recording third data in said corresponding PHB using a fourth said PHB pointer; and assembling said modified header portion using said fourth PHB pointer.

46. The computer readable storage medium of Claim 44, further comprising:
 receiving one or more packets;
 buffering and enqueueing each said packet using said class of service indicator and a plurality of queues; and
 dequeuing each said packet using said class of service indicator.

47. A computer data signal embodied in a carrier wave, comprising computer instructions for:
 receiving a packet, said packet having a header portion, an optional corresponding tail portion, and a class of service indicator;
 switching said packet through a pipelined switch having a plurality of packet header buffers (PHBs), an equal plurality of PHB pointers wherein each said PHB pointer points to a corresponding PHB, and an equal plurality of pipeline stages connected in a sequence, comprising at least a first stage and a last stage, said switching further comprising:
 beginning said sequence in each said stage substantially simultaneously with each other said stage;
 passing data to a next stage circuit in said sequence when every said operation performed by all said stage circuits is completed;
 reading and storing said header in said corresponding PHB using said corresponding PHB pointer; and
 outputting a modified header portion; and
 buffering said modified header portion in a receive buffer manager (RBM), said buffering further comprising:
 joining said modified header portion and said corresponding tail portion to form a modified packet;
 buffering and enqueueing said modified packet using said class of service indicator; and
 dequeuing said modified packet using said class of service indicator.

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48. The computer data signal of Claim 47, wherein said switching further comprises:

recording first data in said corresponding PHB using a second said PHB pointer;

comparing said header portion to a first data structure and determining a leaf pointer using said second PHB pointer;

fetching second data using said leaf pointer to access one or more sets of linked data structures and recording said second data in said corresponding PHB using a third said PHB pointer;

post-processing said header portion using said third PHB pointer and recording third data in said corresponding PHB using a fourth said PHB pointer;

and

assembling said modified header portion using said fourth PHB pointer.

49. The computer data signal of Claim 47, further comprising:

receiving one or more packets;

buffering and enqueueing each said packet using said class of service indicator and a plurality of queues; and

dequeueing each said packet using said class of service indicator.

50. An apparatus for switching packets, said packets having a header portion, a tail portion, and a class of service indicator, comprising:

a pipelined switch comprising a plurality of stage circuits connected in a sequence wherein:

each said stage circuit begins an operation substantially simultaneously with each other said stage circuit;

each said stage circuit passes data when every said operation performed by all said stage circuits is completed;

a last stage circuit that outputs a modified header portion;

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